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United States Patent [19]

Foster et al.

[54] APPARATUS FOR MAINTAINING ONE INTERRUPT MASK REGISTER IN CONFORMITY WITH ANOTHER IN A MANNER INVISIBLE TO AN EXECUTING PROGRAM

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Related U.S. Application Data

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[56] References Cited

U.S. PATENT DOCUMENTS

3,676,861	7/1972	Ruth	340/172.5
4,294,496	10/1981	Murez .	
4.317 180	2/1982	Lies	

[11] Patent Number:

5,551,033

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Aug. 27, 1996

4,381,552 4/1983 Nocilini et al. . 4,458,307 7/1984 McAnlis et al. . 4,461,003 7/1984 Tamaki .

(List continued on next page.)

4,506,323 3/1985 Pusic et al. .

4,523,295 6/1985 Zato.

FOREIGN PATENT DOCUMENTS

53-22345 3/1978 Japan.

OTHER PUBLICATIONS

Zenith Data Systems Corporation, MiniSport HD Owner's Manual, pp. 6–1 through 6–3, 1990.

CLEMENTS, Alan; "Microprocessor Systems Design", 1987, Title pages and p. 117, 246, 247, 353, 354, PWS–Kent Publishing Company, Boston.

Microsoft, MD-DOS, User's Guide, 1986, Title Pages and p. 245.

IBM System/360 Principles of Operation, Eighth Edition (Sep., 1968) Title Pages and pp. 68-83.

Toshiba T1600 "User's Manual" 2d ed.; Title page, pp. 2-1 to 2-3, and pages 2-8 to 2-11, 1987.

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[57] ABSTRACT

A laptop computer system includes a protected mode microprocessor capable of operating in restricted and unrestricted modes, and an arrangement which in response to a predetermined condition saves information from the processor and then forcibly switches the processor to its unrestricted mode of operation. The system includes a first interrupt mask register having a bit for indicating whether an interrupt is to be recognized by the processor, a second interrupt mask register having a bit for indicating whether the interrupt is to be recognized by a further circuit, and an arrangement responsive to a load of the first mask register for conforming the bit of the second mask register to the bit of the first mask register in a manner invisible to an application program being executed by the processor.

9 Claims, 171 Drawing Sheets

